

**UNITED STATES PATENT APPLICATION**

**FLEXIBLE TAPE ELECTRONICS PACKAGING AND METHODS OF  
MANUFACTURE**

**INVENTOR**

**Ajit V. Sathe**

**Schwegman, Lundberg, Woessner & Kluth, P.A.  
1600 TCF Tower  
121 South Eighth Street  
Minneapolis, MN 55402  
ATTORNEY DOCKET SLWK 884.469US1  
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# Flexible Tape Electronics Packaging And Methods of Manufacture

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## Technical Field of the Invention

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The present invention relates generally to electronics packaging. More particularly, the present invention relates to an electronic package that includes an integrated circuit packaged on a flexible tape substrate, and to manufacturing methods related thereto.

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## Information Background of the Invention

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Integrated circuits (ICs) have typically been assembled into electronic packages by physically and electrically coupling them to a substrate made of organic or ceramic material. One or more such IC packages can be physically and electrically coupled to a secondary substrate such as a printed circuit board (PCB) or motherboard to form an "electronic assembly". The "electronic assembly" can be part of an "electronic system". An "electronic system" is broadly defined herein as any product comprising an "electronic assembly". Examples of electronic systems include computers (e.g., desktop, laptop, hand-held, server, etc.), wireless communications devices (e.g., cellular phones, cordless phones, pagers, etc.), computer-related peripherals (e.g., printers, scanners, monitors, etc.), entertainment devices (e.g., televisions, radios, stereos, tape and compact disc players, video cassette recorders, MP3 (Motion Picture Experts Group, Audio Layer 3) players, etc.), and the like.

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In the field of electronic systems there is an incessant competitive pressure among manufacturers to drive the performance of their equipment up while driving down production costs. This is particularly true regarding the packaging of ICs, where each new generation of packaging must provide increased performance while

generally being smaller or more compact in size. As market forces drive equipment manufacturers to produce electronic systems with increased performance and decreased size, IC packaging accordingly also needs to support these requirements.

5 In addition, manufacturers of high-end IC packages, such as processors, are experiencing increasing demand for IC packages mounted in thin, light-weight, and/or resilient packaging, because such packaging is useful for many applications. For example, hand-held electronic systems, such as cellular telephones, palm-top computers, personal digital assistants, calculators, MP3 players, watches, hearing aids, and similar equipment typically requires ICs in thin, light-weight, and/or  
10 flexible packages.

An IC substrate may comprise a number of metal layers selectively patterned to provide metal interconnect lines (referred to herein as "traces"), and one or more electronic components mounted on one or more surfaces of the substrate. The electronic component or components are functionally connected to other elements of  
15 an electronic system through a hierarchy of electrically conductive paths that include the substrate traces. The substrate traces typically carry signals that are transmitted between the electronic components, such as ICs, of the system. Some ICs have a relatively large number of input/output (I/O) terminals (also called "lands"), as well as a large number of power and ground terminals or lands.

20 Surface mount technology (SMT) is a widely known technique for coupling ICs to a substrate. One of the conventional methods for surface-mounting an IC on a substrate is called "controlled collapse chip connect" (C4). In fabricating a C4 package, the electrically conductive terminals or lands of an IC component are soldered directly to corresponding lands on the surface of the substrate using  
25 reflowable solder bumps or balls. The C4 process is widely used because of its robustness and simplicity.

In addition to using SMT to couple an individual IC die to a substrate, it is also well known to use SMT to couple an IC package to a substrate such as a printed circuit board (PCB) or motherboard. Solder bumps, for example, can be employed  
30 between lands on the IC package and corresponding lands on the PCB.

As the internal circuitry of ICs, such as processors, operates at higher and higher clock frequencies, and as ICs operate at higher and higher power levels, the amount of loop inductance produced within IC packages and electronic assemblies can increase to unacceptable levels.

5 For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a significant need in the art for apparatus and methods for packaging an IC that minimize the thickness and weight of the packaging, and that minimize loop inductance within the packaging.

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#### Brief Description of the Drawings

FIG. 1 is a block diagram of an electronic system incorporating at least one electronic assembly with a flexible tape package in accordance with one  
15 embodiment of the invention;

FIG. 2 illustrates a cross-sectional representation of a prior art electronic assembly comprising an IC package mounted on a printed circuit board (PCB);

FIG. 3 illustrates a partially exploded cross-sectional representation of a flexible tape package assembly, taken along dashed line 400 of FIG. 4, including a  
20 die aligned for mounting to a flexible tape substrate overlying a secondary substrate, such as a PCB, in accordance with one embodiment of the invention;

FIG. 4 illustrates a top-view of the flexible tape package assembly shown in FIG. 3, with cut-away portions corresponding to dashed line 300 of FIG. 3;

FIGS. 5-10 together illustrate different stages in a process of fabricating a  
25 flexible tape package assembly, in accordance with one embodiment of the invention, wherein:

FIG. 5 illustrates a top view of a flexible tape substrate having a pattern of lands thereon;

FIG. 6 illustrates a top view of a flexible tape substrate having solder paste  
30 applied to lands on a surface thereof;



organic package substrate. In one embodiment, an IC is mounted on a flexible tape substrate using a ball grid array (BGA) arrangement. Other mounting arrangements, including lead bonding, can be used in conjunction with or in place of BGA mounting. The flexible tape can comprise one or more layers, conductive traces, and patterns of lands. Various embodiments are illustrated and described herein, including methods of fabrication, as well as application of the flexible tape package to an electronic assembly, an electronic system, and a data processing system.

FIG. 1 is a block diagram of an electronic system 1 incorporating at least one electronic assembly 4 with a flexible tape package in accordance with one embodiment of the invention. Electronic assembly 4 has a reduced weight and a reduced thickness or stack height. Electronic assembly 4 can also possess a degree of flexibility, such that it can be bent or molded for particular applications.

Electronic system 1 is merely one example of an electronic system in which the present invention can be used. In this example, electronic system 1 comprises a data processing system that includes a system bus 2 to couple the various components of the system. System bus 2 provides communications links among the various components of the electronic system 1 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

Electronic assembly 4 is coupled to system bus 2. Electronic assembly 4 can include any circuit or combination of circuits. In one embodiment, electronic assembly 4 includes a processor 6 which can be of any type. As used herein, "processor" means any type of computational circuit such as, but not limited to, a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a graphics processor, a digital signal processor (DSP), or any other type of processor or processing circuit.

Other types of circuits that can be included in electronic assembly 4 are a custom circuit, an application-specific integrated circuit (ASIC), or the like, such as, for example, one or more circuits (such as a communications circuit 7) for use in wireless devices like cellular telephones, pagers, portable computers, two-way

radios, and similar electronic systems. Electronic assembly 4 can perform any other type of function.

Electronic system 1 can also include an external memory 10, which in turn can include one or more memory elements suitable to the particular application, such as a main memory 12 in the form of random access memory (RAM), one or more hard drives 14, and/or one or more drives that handle removable media 16 such as floppy diskettes, compact disks (CDs), digital video disk (DVD), and the like.

Electronic system 1 can also include a display device 8, a speaker 9, and a keyboard and/or controller 20, which can include a mouse, trackball, game controller, microphone, voice-recognition device, or any other device that permits a system user to input information into and receive information from the electronic system 1.

Among various embodiments, system 1 could be a hearing aid, a pacemaker, a wristwatch, a pager, a cellular phone, an Internet appliance, a personal digital assistant (PDA), or a palmtop computer. However, many other different embodiments can also take advantage of the relatively low stack height, relatively low weight, and relatively high degree of flexibility of electronic packaging provided by the present invention.

FIG. 2 illustrates a cross-sectional representation of a prior art electronic assembly comprising an IC package mounted on a printed circuit board (PCB). The prior art electronic package includes die 50 having a plurality of signal and power supply lands (not shown) on its lower surface.

The package also includes substrate 60, e.g. an IC package substrate, having a plurality of signal and power supply lands (not shown) on its upper surface that are coupled to corresponding lands of die 50 through bumps or balls 56. IC package substrate 60 is typically formed of an organic material. FR-4 is one type of organic material that is widely used. IC package substrate 60 comprises a plurality of signal and power supply lands 64 on its lower surface. Lands 64 of IC package substrate 60 are coupled to corresponding lands 72 of a secondary substrate, such as printed

circuit board PCB 70, through solder balls or bumps 66. PCB 70 can optionally have lands 74 on its lower surface for attachment to an additional substrate or other packaging structure in the packaging hierarchy.

Regarding the prior art electronic assembly of FIG. 2, the "stack height" 68 is the distance between the upper surface of die 50 and the upper surface of PCB 70. It is desirable to minimize the stack height 68 in order to provide an electronic assembly having minimum thickness and minimal loop inductance. It will be understood that the stack height of a prior art electronic assembly that utilizes a socket arrangement would typically be even greater than the BGA assembly illustrated in FIG. 2.

FIG. 3 illustrates a partially exploded cross-sectional representation of a flexible tape package assembly 100, taken along dashed line 400 of FIG. 4, including a die 110 aligned for mounting to a flexible tape substrate 120 overlying a secondary substrate 130, such as a PCB, in accordance with one embodiment of the invention.

Die 110 can be any type of IC, such as a processor, memory chip, chipset component, or the like.

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In FIG. 3, die 110 comprises a plurality of electronic circuits and signal conductors (not shown) that terminate in lands (not shown) arranged in several rows near the periphery of the bottom surface of die 110 (as viewed in FIG. 3, with die 110 in a flip-chip orientation). Die 110 also comprises a plurality of power and ground conductors (not shown) that terminate in lands (not shown) within the central core region of die 110. The signal and power lands on the lower surface of die 110 can be coupled to corresponding lands, pads, or signal nodes (not shown) on substrate 120 by appropriate connections such as solder bumps or solder balls 112.

SUB D2 7  
Flexible substrate 120, in the embodiment shown in FIG. 3, comprises three layers 121-123. Substrate 120, including layers 121-123, can be formed of a thin, flexible, electrically insulating tape or film. Such films are well known in the tape automated bonding (TAB) art. Such films can be formed of various materials. For



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example, they can be formed of polymeric films, such as polyimide. Other possible materials include polyester, polyparabanic acid, epoxy, and fiberglass.

- In one embodiment, each layer of flexible substrate 120 has a thickness of approximately .20 mm, and the overall thickness of flexible substrate 120, comprising three layers 121-123, is approximately .60 mm. However, in other embodiments, thicker or thinner film could be used. In general, each layer of film can be in the range of approximately .15 mm to .30 mm.

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- Upper layer 123 has formed on its upper surface a plurality of terminals or lands 124 to couple with corresponding pads of IC 110 through bumps 112. Other lands 127 can also be formed on the upper surface of upper layer 123. Lands 127 can be used to couple to corresponding terminals 132 on the upper surface of PCB 130 through wire leads such as lead 140.

- Between upper layer 123 and middle layer 122 are formed a plurality of conductive traces, such as trace 125. Likewise, between middle layer 122 and bottom layer 121 are formed a plurality of conductive traces, such as trace 131. Traces can be formed using any suitable conductive material, such as copper, aluminum, silver, or the like.

Bottom layer 121 has formed on its lower surface a plurality of lands such as lands 128.

- Conductive vias, such as vias 126, can be formed in any layer 121-123, through a subset of layers 121-123, or through all three layers 121-123, to couple traces within different layers 126, or to couple lands such as 124, 127, and 128 to internal traces such as traces 125 and 131.

- While three layers 121-123 are illustrated in the embodiment shown in FIG. 3, fewer or more layers could be used. For example, just one layer could be used. Further, not all layers need to be electrically insulating, because one or more ground planes could be inserted that are formed of any suitable electrically conductive material.

- Substrate 120 can be mounted on a secondary substrate such as PCB 130 by coupling lands 128 of substrate 120 to corresponding terminals 132 on the upper

surface of PCB 130. In one embodiment, lands 128 are coupled to terminals 132 via a ball grid array (BGA) of solder balls (not shown in FIG. 3).

In another embodiment, lands on the upper surface of substrate 120, such as land 127, can be coupled to corresponding lands 132 on the upper surface of PCB 130 through conductive leads or wires, such as lead 140. In yet another embodiment, a combination of BGA and wire lead attachments can be used.

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Substrate 130 can be of any type, such as a printed circuit board (PCB) or card, a motherboard, or any other type of packaging element. Substrate 130 can be a multi-layered substrate or a single-layered substrate. The present invention is not to be construed as limited to any particular type of substrate 130 or to any particular method of coupling substrate 120 to substrate 130. Substrate 130 can optionally have lands (not shown) on its lower surface for attachment to an additional substrate or other packaging structure.

FIG. 30  
The resulting stack height of flexible tape package assembly 100 is significantly less than that of the prior art electronic assembly illustrated in FIG. 2. For example, if a flexible tape substrate 120 having a thickness of .6 mm is used in the embodiment shown in FIG. 3, the resulting overall stack height is approximately 20% less than the stack height of the prior art electronic assembly illustrated in FIG. 2, assuming the thicknesses of the die and die bumps, and the interconnect between the package and the PCB are held constant. Even thinner assemblies can be achieved by using fewer layers within flexible tape package assembly 100.

FIG. 4 illustrates a top-view of the flexible tape package assembly 100 shown in FIG. 3, with cut-away portions corresponding to dashed line 300 of FIG. 3. A first cut-away portion A is to the left of line 101. A second cut-away portion B is between lines 101 and 102. And a third cut-away portion C is to the right of line 102.

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The top-view of flexible tape package assembly 100 shown in portion A includes the top of IC 110 as mounted upon flexible tape package substrate 120 by way of, for example, a surface mount technique, such as a BGA pattern that can

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include lands 124 (shown in dashed lines in portion A, since they are underneath IC 110).

Substrate 120, in turn, can be mounted to a secondary substrate, such as PCB 130, in at least two different ways, both of which are illustrated in portion A, or in a combination of these two ways. A first way is using a BGA pattern that can include lands on the bottom surface of substrate 120, such as lands 128 (shown in dashed lines in portions A-C, since they are underneath substrate 120), that are coupled to corresponding terminals on the upper surface of PCB 130 (such as terminals 132 shown in FIG. 3). Another way is using conductive leads or wires, such as lead 140, which couples a land 127 on the upper surface of flexible tape package substrate 120 to a corresponding terminal 132 on the upper surface of PCB 130.

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The top-view of flexible tape package assembly 100 shown in portion B includes the top of flexible tape package substrate 120, showing a BGA pattern on its upper surface, which includes lands 124.

The top-view of flexible tape package assembly 100 shown in portion C is of the top of layer 121, showing a plurality of conductive traces 131 on the upper surface of layer 121. Also shown (in dashed outline) are lands 128 on the bottom surface of substrate 120. Lands 128 can be coupled to traces 131 using vias such as vias 126.

Flexible tape package substrate 120 has a "conductor region" that is adapted to have mounted thereon an IC, such as IC 110. As used herein, a "conductor region" means a region that can contain vias, traces, and/or lands anywhere within the boundary of the region, as defined for example by dashed outline 519 of FIG. 5 (to be described below). A "conductor region" is typically substantially square or rectangular, though it need not be limited to such shapes. A "conductor region" is distinguishable from a tape automated bonding (TAB) lead-frame conductive pattern, which has conductive leads and pads that are located at the periphery of the pattern, surrounding an IC, but which does not have traces, vias, or lands beneath the IC.

Flexible tape package substrate 120 can include sprockets 104 that are outside the conductor region. Sprockets 104 can be used in conjunction with a suitable transport mechanism (not shown) to facilitate production movement within a high volume manufacturing environment, at least until the flexible tape is  
5 separated or "singulated" into individual IC-mounted tape segments.

FIGS. 5-10 together illustrate different stages in a process of fabricating a flexible tape package assembly, in accordance with one embodiment of the invention.

FIG. 5 illustrates a top view of a flexible tape substrate 500 having a pattern  
10 of lands 524, 527, and 528 thereon. In the embodiment shown in FIG. 5, flexible tape substrate 500 has been formed, and it comprises several layers. Dashed outlines 519 show locations where ICs will subsequently be mounted. Within each dashed outline 519 appears an illustrative pattern of lands, such as land 524, which will be coupled to corresponding pads on the bottom of an IC. In one embodiment,  
15 the pattern is a BGA.

Also seen in FIG. 5 are lands 528 (shown in dashed outline) on the bottom surface of flexible tape substrate 500, which will be used to mount flexible tape substrate 500 to a secondary substrate, such as a PCB. In addition, lands 527 are seen on the upper surface of flexible tape substrate 500, and they can be coupled to  
20 corresponding lands on the PCB using wire leads if desired. Sprockets 504 can be provided to enable transport of the flexible tape substrate 500 through a high volume manufacturing area.

FIG. 6 illustrates a top view of a flexible tape substrate 500 having solder paste applied to lands 524 on a surface thereof. Prior to mounting ICs on flexible  
25 tape substrate 500, solder paste can be applied to all exposed lands on flexible tape substrate 500, or alternatively just to lands 524 (as indicated by cross-hatching) to which the ICs will be mounted. The ICs can have a bump or ball pattern already applied. Alternatively, a ball pattern could be applied to lands 524 of flexible tape substrate 500.

FIG. 7 illustrates a top view of a flexible tape substrate 500 with dice 520 mounted on a surface thereof. Dice 520 can be mounted using a BGA arrangement in which solder bumps or balls on the lower surfaces of dice 520 are coupled using, for example, a solder reflow process, to corresponding lands 524 (shown in dashed outline) on the upper surface of flexible tape substrate 500.

FIG. 8 illustrates a bottom view of a segment of flexible tape IC package 501 having solder balls on a surface thereof. Seen in dashed outline 520 is an IC mounted on the upper surface of flexible tape IC package 501. Prior to this stage in the process, flexible tape substrate 500 has been segmented or "singulated" into individual tape segments. After singulation, the individual flexible tape substrate segments, referred to hereinafter as flexible tape IC packages 501, are typically placed into transport carriers or trays for subsequent testing and possibly other manufacturing and shipping operations. Next, solder balls are formed on corresponding lands 528.

FIG. 9 illustrates a top view of a portion of a secondary substrate 530, such as a PCB, having a flexible tape IC package 501 mounted thereon. Flexible tape IC package 501 includes IC 520. Also shown is a pattern of lands 528 (in dashed outline) on the bottom of flexible tape IC package 501, which pattern can be a BGA. In FIG. 9, flexible tape IC package 501 has been aligned with PCB 530, and lands 528 have been coupled to corresponding terminals (not shown) on PCB 530, e.g. using a solder reflow process.

FIG. 10 illustrates a top view of a portion of the secondary substrate 530 and flexible tape IC package 501 of FIG. 9, with leads 540 mounted. As mentioned earlier, flexible tape IC package 501 can be mounted using solely a BGA pattern, using solely lead bonding, or using a combination of BGA and lead bonding. If lead bonding is used, leads 540 are coupled between lands 527 on the upper surface of flexible tape IC package 501 and corresponding terminals 532 on the upper surface of PCB 530.

FIG. 11 is a flow diagram illustrating a method 600 of fabricating a flexible IC package substrate, in accordance with one or more embodiments of the invention.

5 In 602, a thin, flexible substrate is provided. The substrate is formed of material such as a polymeric film, polyimide, polyester, polyparabanic acid, epoxy, fiberglass, or a combination of these materials. The substrate has a "conductor region" (as defined earlier) adapted to mount an IC. The substrate can include from 1 to N layers. The substrate can also include, if desired, sprocket holes located outside the "conductor region".

10 In 604, a plurality of traces are formed in the conductor region. The traces can be formed on different layers, or they can be formed on one layer.

In 606, a plurality of lands are formed that are coupled to certain traces of the plurality of traces. The lands can be formed on opposite sides of the substrate, or on just one side of the substrate. In one embodiment, the lands are arranged in  
15 one or more ball grid arrays (BGAs).

In 608, solder bumps or balls are formed on the plurality of lands. The solder balls can be formed on different groups of the lands. For example, a first set of lands can be covered with solder balls in order to couple the substrate to an IC, and a second set of lands can be covered with solder balls in order to couple the  
20 substrate (including IC) to a PCB. The process ends at 610.

FIGS. 12A and 12B together form a flow diagram illustrating a method 700 of fabricating an electronic assembly, in accordance with one or more embodiments of the invention.

25 In 702, a thin, flexible substrate is provided. The substrate is formed of material such as a polymeric film, polyimide, polyester, polyparabanic acid, epoxy, fiberglass, or a combination of these materials. The substrate has a "conductor region" (as defined earlier) that includes a plurality of traces and a plurality of lands coupled to certain traces. The substrate can include from 1 to N layers, each comprising a plurality of traces in the "conductor region". The lands can be formed

on different layers. The substrate can also include, if desired, sprocket holes located outside the "conductor region".

In 704, solder balls are formed on a first set of lands, which can be a ball grid array (BGA).

5 In 706, pads of an IC are coupled to corresponding ones of the first set of lands using, for example, a solder reflow operation.

In 708, the substrate is mounted on an additional substrate, such as a PCB. Either or both of the following techniques can be used: (1) use a BGA pattern between the substrate and the PCB, by forming solder balls on a second set of the  
10 lands, and coupling ones of the second set of lands to corresponding terminals on the PCB; (2) use leads between the substrate and the PCB, by coupling leads, such as wires, between corresponding ones of a third set of lands and additional terminals of the PCB. The process ends in 710.

The operations described above with respect to the methods illustrated in  
15 FIGS. 11, 12A, and 12B can be performed in a different order from those described herein. Also, it will be understood that while an "end" block is shown in FIGS. 11 and 12B, these methods can be performed continuously.

#### Conclusion

20 The present invention provides for a lightweight electronic package, in several different embodiments, and for methods of manufacture thereof, that minimize the thickness of the package, and that offer some degree of flexibility and/or of moldability. Loop inductance within the package is also reduced, because  
25 conductive paths through the flexible tape substrate are shorter than they are through an organic substrate.

30 An electronic system and/or data processing system that incorporates one or more electronic assemblies that utilize the present invention can be produced in configurations having reduced thickness and weight, and with enhanced flexibility

and electronic performance, and such systems are therefore more commercially attractive.

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5 As shown herein, the present invention can be implemented in a number of different embodiments, including an electronic package substrate, an electronic package, an electronic system, a data processing system, one or more methods of fabricating a flexible tape package, and one or more methods of fabricating a flexible tape package assembly. Other embodiments will be readily apparent to those of ordinary skill in the art. The elements, materials, geometries, dimensions, and sequence of operations can all be varied to suit particular packaging requirements.  
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11 For example, while an embodiment of an IC is shown in which signal traces are provided around the periphery and in which power supply traces are provided at the die core, the invention is equally applicable to embodiments where signal traces and power supply traces are provided anywhere on the die.

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